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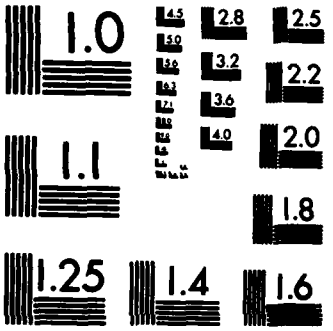

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REPORT DOCUMENTATION PAGE

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1. REPORT NUMBER: ARO 16813.1-EL	2. GOVT ACCESSION NO.: N/A
3. RECIPIENT'S CATALOG NUMBER: N/A	
4. TITLE (and Subtitle): Monolithic Integrated Antenna Systems	5. TYPE OF REPORT & PERIOD COVERED: Final Report, August 1980 - February 1984
	6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s): P. J. Burlingame; R. J. Stockton	8. CONTRACT OR GRANT NUMBER(s): DAAG29-80-C-0132
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Ball Aerospace Systems Division, P.O. Box 1062, Boulder, CO 80306	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS: U. S. Army Research Office, Post Office Box 12211, Research Triangle Park, NC 27709	12. REPORT DATE: 8 June 1984
	13. NUMBER OF PAGES: 8
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)	15. SECURITY CLASS. (of this report): Unclassified
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

NA

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18. SUPPLEMENTARY NOTES

The view, opinions, and/or findings contained in this report are those of the author(s) and should not be construed as an official Department of the Army position, policy, or decision, unless so designated by other documentation.

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Monolithic Phased Array
Microstrip Phased Array
Microstrip Antenna
Monolithic Microwave Integrated Circuit (MMIC)
High Resistivity Silicon

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A 4 x 4, 17.5 GHz Monolithic Phased Array fabricated on high resistivity silicon is described. This approach combines microstrip antenna elements, beam lead PIN diodes and silicon integrated circuit technology to replace labor intensive hybrid circuit construction techniques with low cost, repeatable integrated circuit processes. Preliminary test data from two hardware iterations is presented. Although the program is formally concluded, additional testing is still being conducted to characterize overall array performance.

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This program developed a 17.5 GHz monolithic phased array (MPA) on high resistivity silicon. A monolithic array combines microstrip circuitry and radiators, microwave active devices and integrated circuit fabrication technology to create a "phased array on a chip" with no discrete components. All of the devices and components are fabricated in-situ at the wafer level. Although the silicon substrate severly limits performance at Ku-Band, it is a low cost, first generation prototype which logically preceded GaAs. Monolithic phased arrays on semi-insulating GaAs are superior due to lower substrate losses and the ability to implement active aperture concepts up to 60 GHz using FET amplifiers and phase shifters. However, they are substantially more expensive as a result of the sub-micron feature sizes and attendant processing requirements.

A photograph of the silicon monolithic phased array is shown in Figure 1. It consists of a 4 x 4 array of microstrip elements on a 1.4 inch x 1.4 inch x .015 inch substrate. A 3-bit phase shifter consisting of branch-line hybrid 180^{o} and 90^{o} bits and a loaded line 45^{o} bit is integrated at the element level. The feed network, bias chokes and bias lines are also included on the aperture surface. The planar topology of the circuit layout does not require any crossovers. The phase shifter switching devices are beam-lead type PIN diodes.

Array construction began with the monolithic fabrication of the PIN diodes on a 2-inch diameter, 5000 ohm-cm silicon wafer. The 96 diodes were fabricated in the desired locations with specific orientations as shown in Figure 2. The second and final step defined the thin-film metallization pattern for the radiating elements, feed network, phase shifter circuitry, diode interconnects and bias lines. The entire wafer was metallized and then coated with photoresist. Using standard photolithographic techniques and the mask shown in Figure 3, the thin-film gold is selectively removed leaving the completed array metallization pattern shown in Figure 1.

Initial measurements of the far-field patterns resulted in a spoiled beam as shown in Figure 4. The beam shape and position was relatively independent of the phase shifter settings. Network analyzer measurements of the array indicated that there was heavy coupling between the input feed line and the

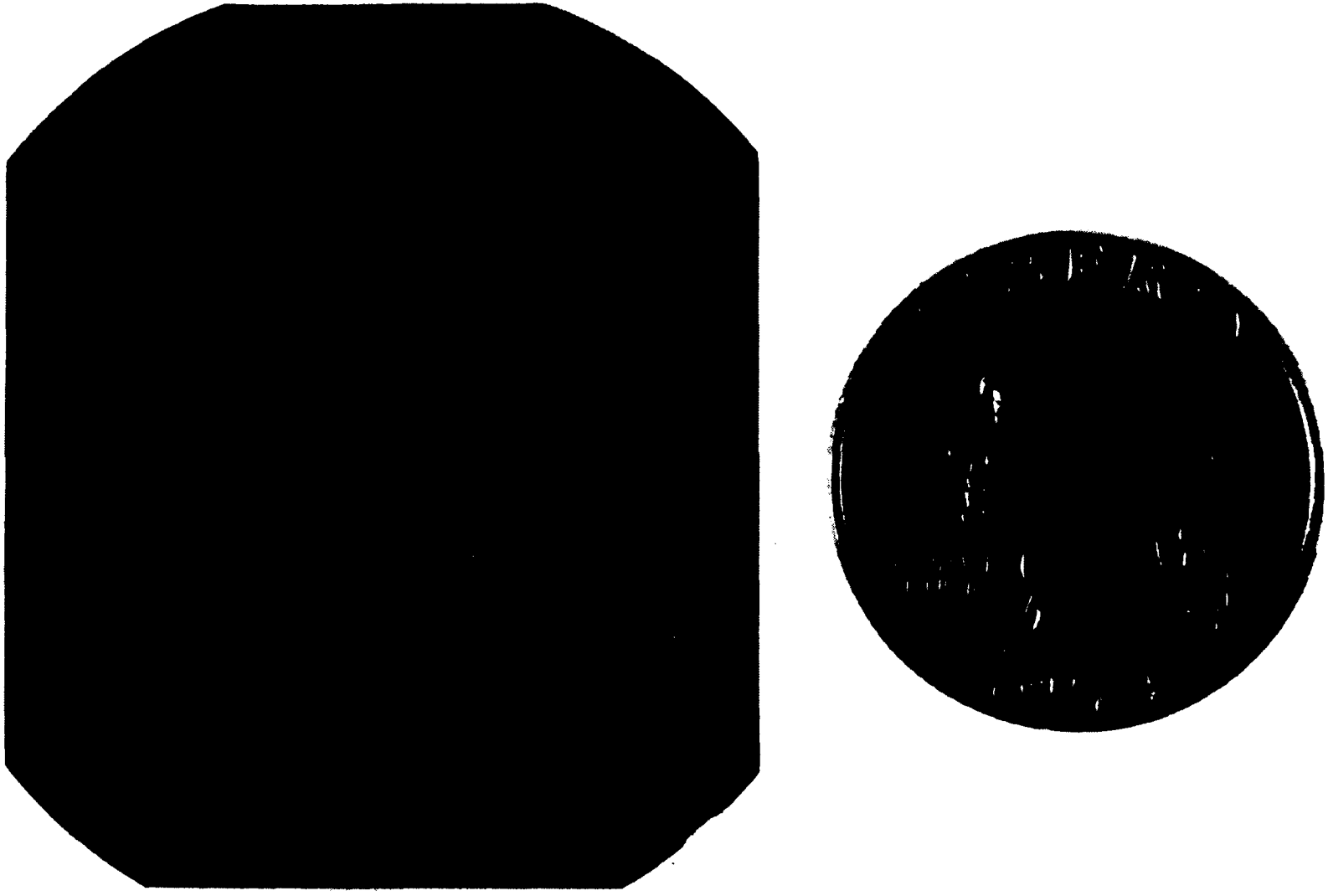

Figure 1. A 4 x 4, 17.5 GHz Monolithic Phased Array on High Resistivity Silicon.

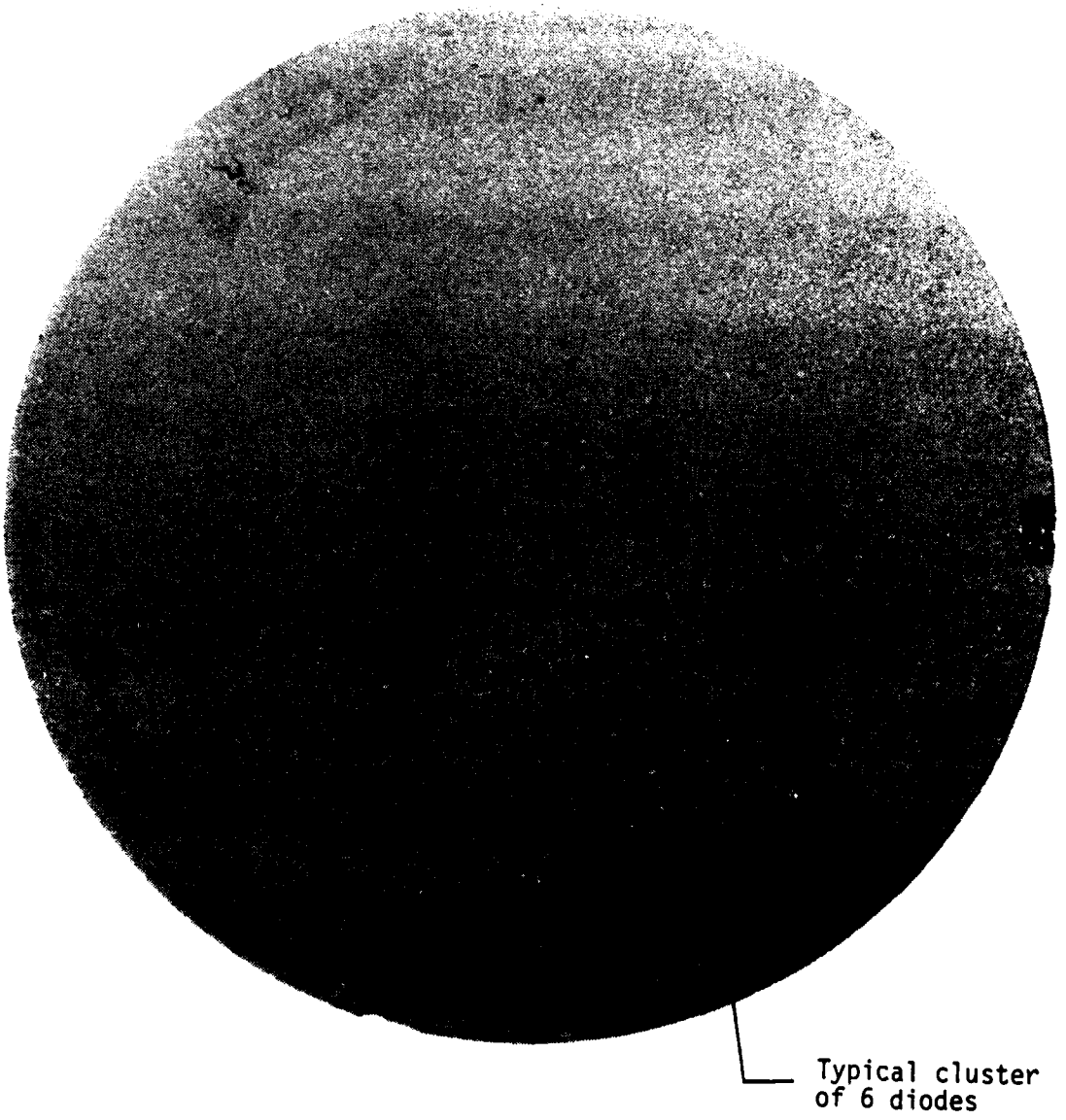

Figure 2. 2-inch Diameter Silicon Wafer Containing 16 Groups of 6 Monolithic Beam Lead Type Diodes.

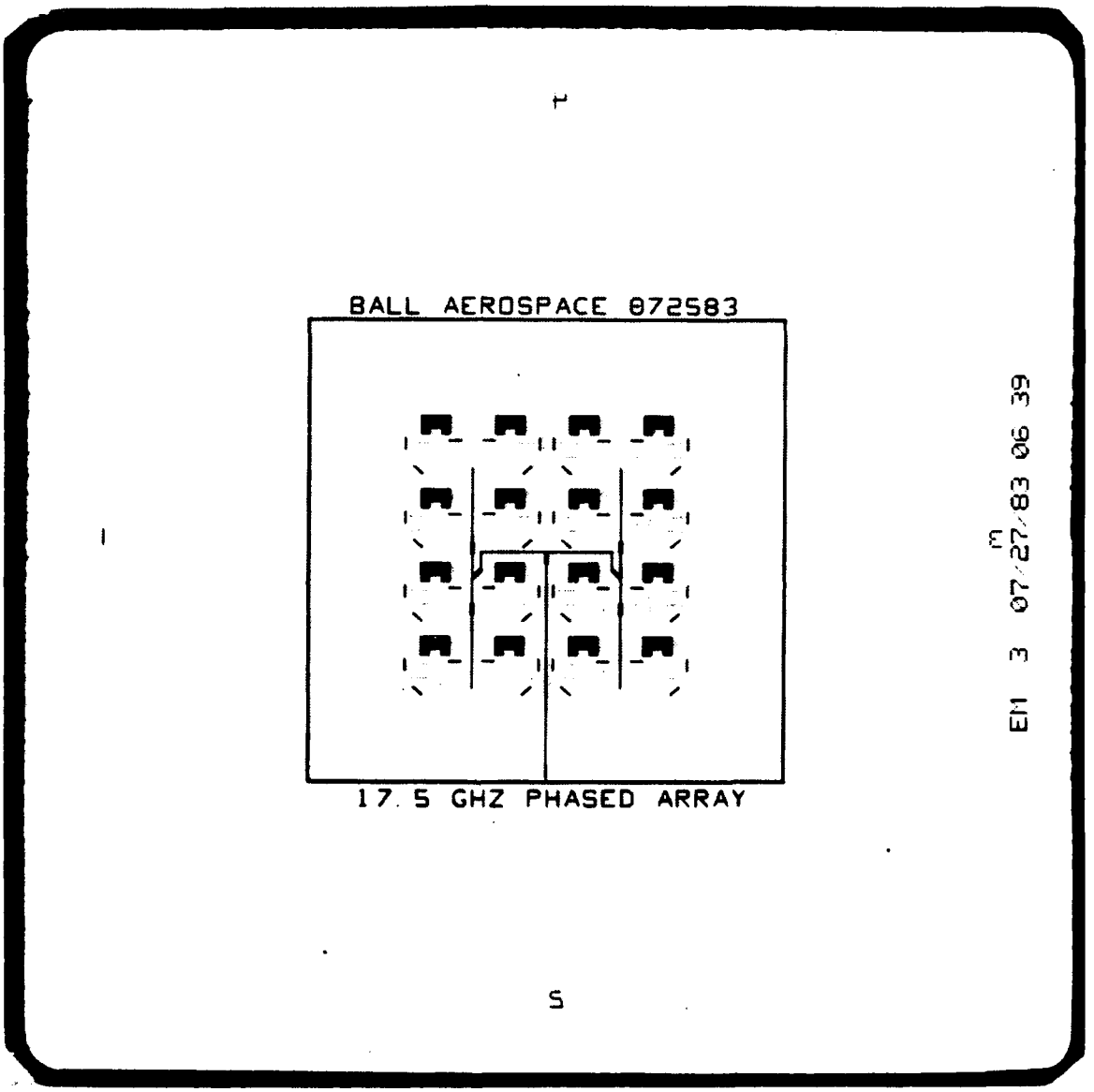

Figure 3. Metallization Mask for Elements, Feed Network, Phase Shifter Circuitry and Bias Lines.

adjacent parallel bias lines shown in Figure 1. As a result the major portion of the input power was radiated from the bias line discontinuities.

To solve this problem, the array was modified by directly feeding the central binary power divider. A hole was ultrasonically milled through the substrate to accommodate the center pin of a rear mounted connector. The planar, monolithic input feed line was carefully etched away. The input VSWR for this configuration was less than 2:1 between 17 and 18 GHz. Far-field patterns for this array configuration confirmed that the coupling problem had been significantly reduced. Different phase shifter settings resulted in distinct and repeatable patterns. However, the patterns still contained a poorly defined main beam as shown in Figure 5. Investigation of the test set-up indicated that the phase shifter controllers for the rows and columns had been interchanged. This problem caused serious phase errors since the design of the array contained a 180^{o} phase offset in rows 1 and 4 with respect to rows 2 and 3. Therefore, in order to form a broadside beam, a 180^{o} phase delay is required in the central rows. The row-column reversal introduced incorrect phase settings as illustrated in Figure 6.

The phase shifter controller is easily modified to correct this problem. Upon completion of these changes, a final set of patterns will be taken to characterize overall array performance.

Although actual performance parameters are unknown since the array is still under test, the calculated performance projections are summarized in Table 1. The low efficiency is primarily due to dissipative losses in the silicon substrate material which degrades to a post-processing resistivity of 2500 ohm-cm. For comparison, semi-insulating GaAs retains its 10^{6} - 10^{8} ohm-cm resistivity even after processing.

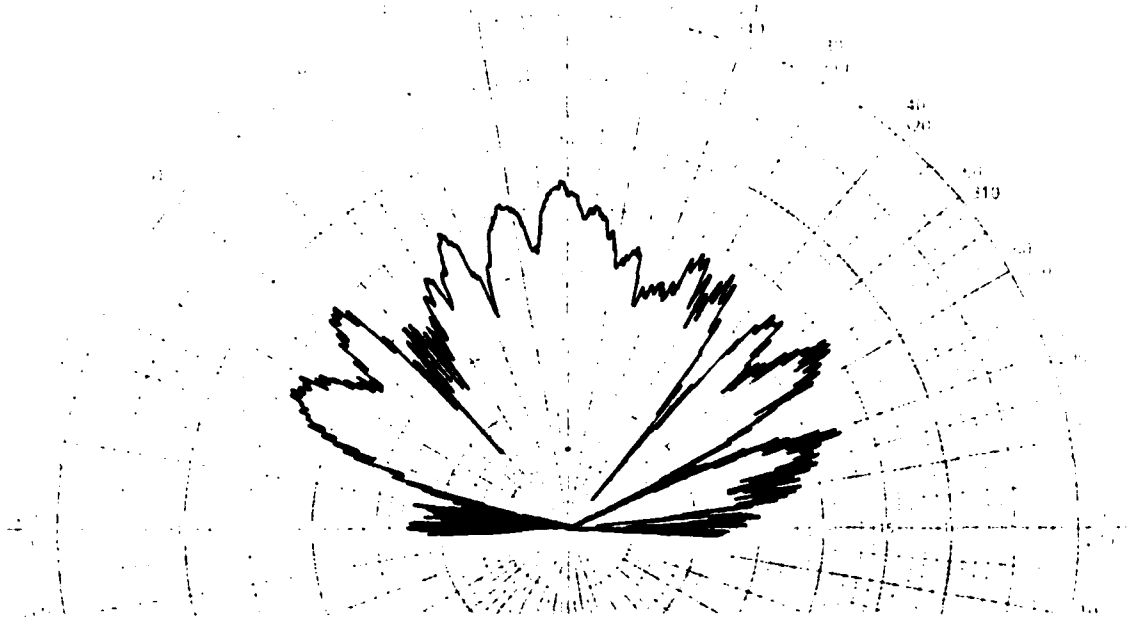

Figure 4. Initial H-plane Far-Field Pattern.

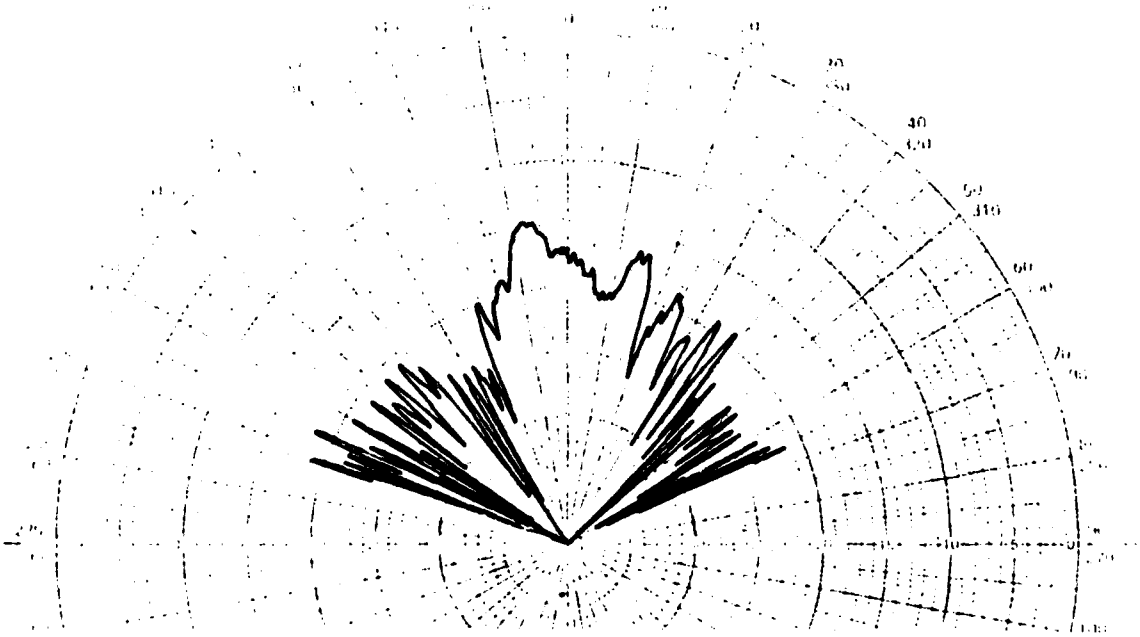

Figure 5. H-plane Far-Field Pattern with the Phase Relationship Shown in Figure 6.

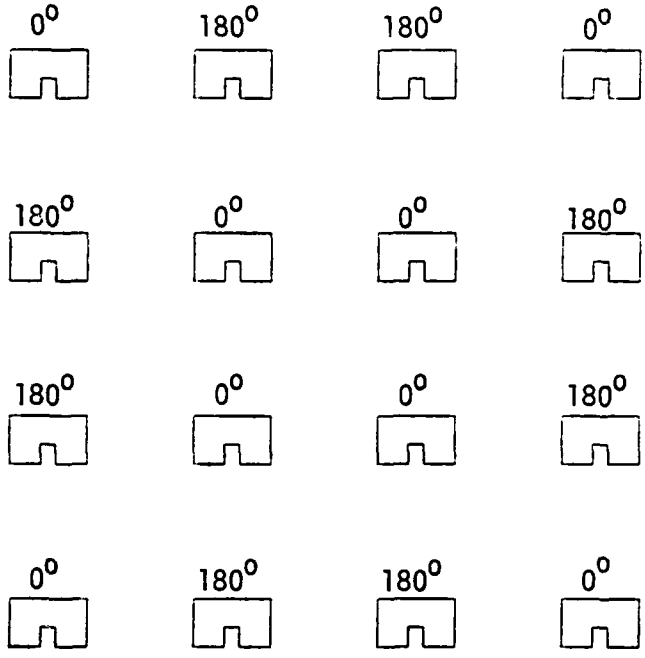

Figure 6. Relative Phases Between Array Elements for a Broadside Beam Due to Row-Column Reversal in Controller.

Table 1

4x4 Silicon MPA Performance Projections

Frequency	17.5 GHz
Bandwidth	>5%
Input VSWR	<2.0:1
Scan Coverage	110^{o} Cone Angle
HPBW	32^{o} (broadside)
Gain	11 dBi (broadside)
Efficiency	25%
Phase Shifter Loss	3 dB

The weight of the array substrate is less than 1.2 grams.